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cont.

a common source wiring provided over said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring provided over said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less.

2. (Twice Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a driver circuit in said active matrix type display device;

a common gate wiring provided over said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring provided over said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided over said insulating surface and connected with said two transistors at the other of the source and drain of each of said two transistors,

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wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less.

3. (Twice Amended) An active matrix type display device comprising:

at least two transistors provided on an insulating surface in a buffer circuit in said active matrix type display device;

a common gate wiring provided over said insulating surface and connected with said two transistors at gate electrodes of said two transistors;

a common source wiring provided over said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and

a common drain wiring provided over said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and containing oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less, and each of said channel-forming regions not having linear defects or surface defects.

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8. (Twice Amended) An active matrix type display device comprising:
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at least two transistors provided on an insulating surface in a driver circuit in said active matrix type display device;
a common gate wiring provided on said insulating surface and connected with said at least two transistors at gate electrodes of said at least two transistors;
a common source wiring provided on said insulating surface and connected with said at least two transistors at one of source and drain of each of said at least two transistors; and
a common drain wiring provided on said insulating surface and connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,
wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and
wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively, each of said channel-forming regions containing carbon and nitrogen at a concentration of 5×10^{18} cm³ or less, respectively, and containing oxygen at a concentration of 5×10^{19} cm³ or less, and each of said channel-forming regions not having linear defects or surface defects.

Please add new claims 76-99 as follows.

F3
76.(New) The device of claim 1 wherein said channel-forming region does not have linear defects or surface defects.

77.(New) The device of claim 2 wherein said channel-forming region does not have linear defects or surface defects.